Abstract

A method and apparatus for modeling using a hardware-software co-verification environment. The present invention allows the designer to simulate a direct interface with the micro-controller. An instruction set simulator is coupled to a simulator circuit to determine if the hardware design is correct. Specifically, the instruction set simulator acts as a "master" to the simulator circuit, thus providing a faster simulation environment. The simulator circuit contains a bus functional model, a hardware model, transfer memory, and the hardware design to be tested. The hardware model is designed to emulate a micro-controller. By disabling the processor within the hardware model, the speed of the simulation is restricted only by the speed of the instruction set simulator or the hardware design. Furthermore, the hardware design may be uncoupled from the simulatorcircuit in order to initialize the operating system.